

RAMAKRISHNA MISSION VIDYAMANDIRA

(Residential Autonomous College under University of Calcutta)

B.A./B.SC. FIRST SEMESTER EXAMINATION, DECEMBER 2012

FIRST YEAR

COMPUTER SCIENCE (Honours)

Date : 14/12/2012

Time : 11 am – 2 pm

Paper : I

Full Marks : 75

Use separate answer-book for each group

Group – A

(Answer any two questions)

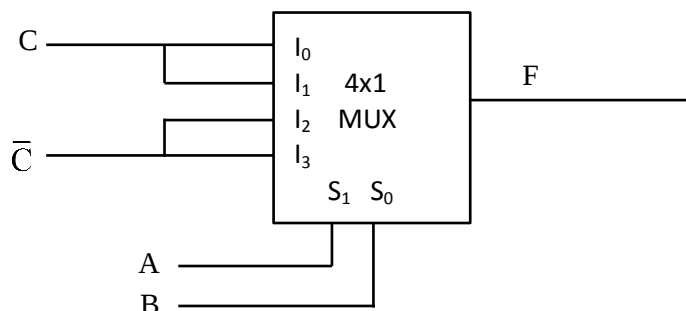
1. a) Translate the following English sentences into Propositional logic formulas:
 - i) Many will show up only if Fred shows up.
 - ii) Many will be extremely happy but Fred will be surprised. 2+2
- b) What do you mean by Tautology? Check whether the following expression is a Tautology:
 $(p \Rightarrow (q \wedge r)) \Leftrightarrow (p \Rightarrow q) \wedge (p \Rightarrow r).$ 2+2½
- c) i) Define wff in Predicate calculus.
ii) Write the following English statement in terms of Predicate logic formulas:
“Some sleepy students didn’t answer any questions”. 2+2
2. a) Find out the relation between the number of bits to represent information and the number of parity bits to generate a Hamming code. If the information bits are 1011_2 , generate the corresponding Hamming code. 2+3
- b) Convert the Gray code 110011 to its binary equivalent. 2
- c) Using algebraic methods, prove the following two versions of Consensus Theorem: 2+2
 - i) $XY + \bar{X}Z + YZ = XY + \bar{X}Z$
 - ii) $(X + Y)(\bar{X} + Z)(Y + Z) = (X + Y)(\bar{X} + Z)$

X, Y and Z are three Boolean variables.
- d) Represent the Boolean expression $Y = A + B\bar{C}$ using NAND gates only. 1½
3. a) Given a quadratic equation $5x^2 + 50x + 125 = 0$ in a base r . The roots of the equation are -8 & -5 in base 10. Find the value of base r . 5
- b) “Boolean algebra doesn’t ensure realization of minimized Boolean function. But still some point of time it will be used to realize minimization of Boolean function.” – Proof or disproof the above comment with proper justification. 2½
- c) What do you mean by Veitch diagram? How it is used to minimize a Boolean function? State the limitation of this diagram. 1+2+2

Group – B

(Answer any five questions)

4. a) What is the logic realized by the circuit shown in the figure below: 3



- b) What are control and status registers? 2
- c) Briefly discuss various stages of instruction cycle using instruction cycle state diagram. 5
5. a) Realize a J-K flip-flop using a D flip-flop. 6
- b) Illustrate the working principle of a 4-bit serial adder. 4
6. a) Write down the instructions in zero-address format and three-address format to execute the following operation: $X = A * (B - C)$. 2+2
- b) Why is it necessary to have different addressing modes of any assembly language program? 2
- c) Make a comparative study between RISC architecture and CISC architecture. 4
7. a) Express $(0.239)_{10}$ in Excess-64 base 2 representation. 3
- b) Perform $(8 \div 3)$ using Booth's restoring division algorithm. 5
- c) What are the basic design methods of hardwired control unit? 2
8. a) Design a 4×4 RAM using 1×1 RAM cells. 3
- b) State differences of SRAM and DRAM. 2
- c) What is cache coherency? 2
- d) For a three level memory system, let T_1 , T_2 and T_3 be the effective access times of the levels respectively. Given $T_2 = 2T_1$, $T_3 = 3T_1$ and hit ratio $h_1 = h_2 = 0.9T_1$. Calculate average memory access time in terms of T_1 . 3
9. a) Design a full-subtractor using necessary multiplexer(s). 5
- b) What do you mean by the race-around condition? With a proper diagram, explain the way this condition is avoided using a master-slave flip-flop. 2+3
10. a) Design the logic circuit of a 4-bit parallel adder-subtractor. Also explain its function. 3+3
- b) Design a logic circuit which can convert a 3-bit number to its 2's complement form. 4

